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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/580,619	05/24/2006	Raymond J.E. Hueting	GB03 0213 US1	5566
65913	7590	08/06/2009	EXAMINER	
NXP, B.V. NXP INTELLECTUAL PROPERTY & LICENSING M/S41-SJ 1109 MCKAY DRIVE SAN JOSE, CA 95131			RAO, SHRINIVAS H	
			ART UNIT	PAPER NUMBER
			2814	
			NOTIFICATION DATE	DELIVERY MODE
			08/06/2009	ELECTRONIC

**Please find below and/or attached an Office communication concerning this application or proceeding.**

The time period for reply, if any, is set in the attached communication.

Notice of the Office communication was sent electronically on above-indicated "Notification Date" to the following e-mail address(es):

ip.department.us@nxp.com

**Office Action Summary**

<b>Application No.</b> 10/580,619	<b>Applicant(s)</b> HUETING ET AL.	
<b>Examiner</b> STEVEN H. RAO	<b>Art Unit</b> 2814	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

**Period for Reply**

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

**Status**

- 1)  Responsive to communication(s) filed on 19 May 2009.
- 2a)  This action is **FINAL**.
- 2b)  This action is non-final.
- 3)  Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

**Disposition of Claims**

- 4)  Claim(s) 1 and 3-14 is/are pending in the application.  
4a) Of the above claim(s) \_\_\_\_\_ is/are withdrawn from consideration.
- 5)  Claim(s) \_\_\_\_\_ is/are allowed.
- 6)  Claim(s) 1 and 3-14 is/are rejected.
- 7)  Claim(s) \_\_\_\_\_ is/are objected to.
- 8)  Claim(s) \_\_\_\_\_ are subject to restriction and/or election requirement.

**Application Papers**

- 9)  The specification is objected to by the Examiner.
- 10)  The drawing(s) filed on \_\_\_\_\_ is/are: a)  accepted or b)  objected to by the Examiner.  
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).  
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11)  The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

**Priority under 35 U.S.C. § 119**

- 12)  Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).  
a)  All   b)  Some \*   c)  None of:  
1.  Certified copies of the priority documents have been received.  
2.  Certified copies of the priority documents have been received in Application No. \_\_\_\_\_.  
3.  Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

\* See the attached detailed Office action for a list of the certified copies not received.

**Attachment(s)**

- 1)  Notice of References Cited (PTO-892)
- 2)  Notice of Draftsperson's Patent Drawing Review (PTO-948)
- 3)  Information Disclosure Statement(s) (PTO/SB/08)  
Paper No(s)/Mail Date \_\_\_\_\_.
- 4)  Interview Summary (PTO-413)  
Paper No(s)/Mail Date \_\_\_\_\_.
- 5)  Notice of Informal Patent Application
- 6)  Other: \_\_\_\_\_.

## DETAILED ACTION

### ***Continued Examination Under 37 CFR 1.114***

1. A request for continued examination under 37 CFR 1.114, including the fee set forth in 37 CFR 1.17(e), was filed in this application after final rejection. Since this application is eligible for continued examination under 37 CFR 1.114, and the fee set forth in 37 CFR 1.17(e) has been timely paid, the finality of the previous Office action has been withdrawn pursuant to 37 CFR 1.114.

2. Applicant's submission filed on May 19,2009 has been entered and forwarded to the Examiner on May 21.2009.

Therefore claims 1, 12 and 13 as amended by the amendment and claims 3 to10 and 14 as previously recited are currently pending in the application.

Claim 2 was previously cancelled.

### ***Information Disclosure Statement***

To date no IDS has been filed in this case.

### ***Claim Rejections - 35 USC § 103***

3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

4. Claims 1and 3 to 14 are rejected under 35 U.S.C. 103(a) as being unpatentable over Fujishima ( U.S. Patent No. 5,981,996 herein after Fujishima, previously applied) in view of Kocon ( EPA Patent No. 1054451, herein after Kocon,also cited by Applicants’).

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With respect to claim 1 Fujishima describes an insulated gate field effect transistor, comprising:

a source region of first conductivity type (Fujishima fig.I, 104) ; a body region of a second conductivity type opposite to the first conductivity type adjacent to the source region ( Fujishima fig.1,111) ; a drift region of exclusively the first conductivity type adjacent to the body region ( Fujishima fig.1,102) ; a drain region of the first conductivity type adjacent to the drift region, ( Fujishima fig I, 109) so that body and drift regions are arranged between the source and drain regions (Fujishima fig.I), the drain region being of higher doping density than the drift region (Fujishima col. 10 line 10 and inherent because drain region below drift and therefore higher doping density).

Fujishima does not specifically mention the presently newly added limitation “wherein the region between the body region and the drain region is made up of exclusively the drift region of exclusively the first conductivity type.

However Kocon, a patent from the same field of endeavor , describes in figure 2 and . Paras 0017 to 0021 ,etc. the region between the body region and the drain region is made up of exclusively the drift region of exclusively the first conductivity type to greatly reduce the unit cell dimension so as to reduce the on resistance thereby improving the trade-off relation between the breakdown voltage and the on resistance.

Therefore it would have been obvious to one of ordinary skill in the art at the time of the invention to include Kocon’s the region between the body region and the drain region is made up of exclusively the drift region of exclusively the first conductivity type as described in figure 2 and paras 0017 to 0021, etc. in Fujishima’s device . The motivation for the above combination is to greatly reduce the unit cell dimension so as to reduce the on resistance thereby improving the trade-off relation between the breakdown voltage and the on resistance and provide a simpler manufacturing process.

The remaining limitations of Claim 1 are :

and insulated trenches extending from the source region through the body region and into the drift region each trench having sidewalls and including an

insulator on the sidewalls ( Fujishima figs.I,4 105, insulator-406), and a conductive gate electrode between the insulating sidewall, (Fujishima fig. 1,107) wherein the base of each trench is filled with an insulator plug adjacent to substantially all of the length of the drift region between the body region and drain region .( Fujishima to the extent understood- fig. 1, 112) and the respective gate electrode is provided in the trench over the plug adjacent to the source and body (Fujishima fig.1 107).

*With respect to claim 3 Fujishima describes an insulated gate field effect transistor according to claim 1 wherein the doping concentration in the body region is in the range of about  $0.5 \times 10^{17}$  cm<sup>3</sup> to about  $3 \times 10^{17}$  cm<sup>-3</sup> and the doping concentration in the drift region) is in the range about  $1 \times$*

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1015 cm<sup>-3</sup> to about 2x 10<sup>17</sup> cm<sup>-3</sup>. (Fujishima col. 8 lines 45,46-49,54; col. 9-55 ;10-5,10).

*With respect to claim 4 Fujishima describes an insulated gate field effect transistor according to claim 1 wherein the plug is of dielectric filler filling the trench between the insulator on the sidewalls adjacent to the drain region. ( Fujishima Fig. 1,106 ).*

*With respect to claim 5 Fujishima describes an insulated gate field effect transistor according to claim 1 having a semiconductor body (Fujishima fig.I, 111 ) having opposed first-(Fujishima fig. 1 ) second major surfaces (Fujishima fig. 1), wherein the source region (Fujishima 104) is at the first major surface over the region, the body region (Fujishima 111 )is over the drift region (Fujishima 102) and the drift region (Fujishima 102)is over the drain region (Fujishima 109), and the trench (Fujishima 105)extends from the first major surface towards the second major surface through the source (Fujishima 104), body (Fujishima 111 ) and drift (Fujishima 102) regions.*

*With respect to claim 6 Fujishima describes an insulated gate field effect transistor according to claim 5 having a plurality of cells each cell having a source region at centre of the cell surrounded by the insulated trench. (Fujishima col. 12 line 61 ).*

*With respect to claim 7 Fujishima describes an insulated gate field effect transistor according to claim 6 wherein the cells have a hexagonal geometry. (well known in the art e.g. Hark also cited by applicants in their IDS).*

*With respect to claim 8 Fujishima describes an insulated gate field effect transistor according to claim 6 wherein the trench (Fujishima figs. 105 ) has gate oxide (Fujishima Fig.106) on the sidewalls, and the trench adjacent to the drift region is filled with filler oxide between the gate oxide (Fujishima fig. 112) on the sidewalls on either side of the trench. (Fujishima fig.112 ).*

*With respect to claim 9 Fujishima describes an insulated gate field effect transistor according to claim 5 having a plurality of cells (Fujishima col. 12 line 61 ) arranged as stripes across the first major surface (Fujishima Fig. I) with alternating trenches (Fujishima 105) and source regions (Fujishima 104).*

With respect to claim 10 Fujishima describes an insulated gate field effect transistor according to claim 6 wherein the cell pitch is in the range of about 0.2 microns to about 0.7 microns. (Fujishima col. 9 lines 35 to col. 10 lines 19).

With respect to claims 11 and 12 Fujishima describes an insulated gate field effect transistor according to claims 1 /11 wherein the doping concentration in the drift region is non-uniform.( it is inherent that the portion of the drift region in Fujishima figs., e.g. fig.1 at a higher level "i.e. adjacent drift region have lower doping concentration than the

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portion of the drift region at a lower level ( adjacent to the drain region 109, see also response to applicants arguments section in final rejection, Kocon paras 0020, 0024, claims 2,3 etc.).

With respect to claim 13 Fujishima describes an insulated gate field effect transistor according to claim 12 wherein the non-uniform doping concentration in the drift region is linearly graded from the higher doping concentration adjacent to the drain region to the lower doping concentration adjacent to the body region..( it is inherent that the portion of the drift region in figs., e.g. Fujishima fig.1 at a higher level "i.e. adjacent drift region have higher doping concentration than the portion of the drift region at a lower level will have lower concentration i.e. linearly graded adjacent to the drain region 109, see also response to applicants arguments section below Kocon paras 0020, 0024, claims 2,3 etc.).

With respect to claim 14 Fujishima describes an insulated gate field effect transistor according to claim 11 wherein the doping concentration in the body region is in the range of about  $0.5 \times 10^{17} \text{ cm}^{-3}$  to about  $3 \times 10^{-7} \text{ cm}^{-3}$ , and the doping concentration in the drift region is in the range of about  $1 \times 10^{-5} \text{ cm}^{-3}$  to about  $2 \times 10^{-7} \text{ cm}^{-3}$ . (rejected for reasons under claim 3 above - Fujishima col. 8 lines 45,46-49,54; col. 9-55 ;10-5,10 and response to arguments section in the final rejection).

### ***Response to Arguments***

5. Applicant's arguments with respect to claims 1 to 14 are have been considered but are moot in view of the new ground(s) of rejection.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to STEVEN H. RAO whose telephone number is (571)272-1718. The examiner can normally be reached on 8.30-5.30.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Wael Fahmy can be reached on 571-272-1714. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

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Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/Steven H Rao/  
Examiner, Art Unit 2814